

**FIG. 1**

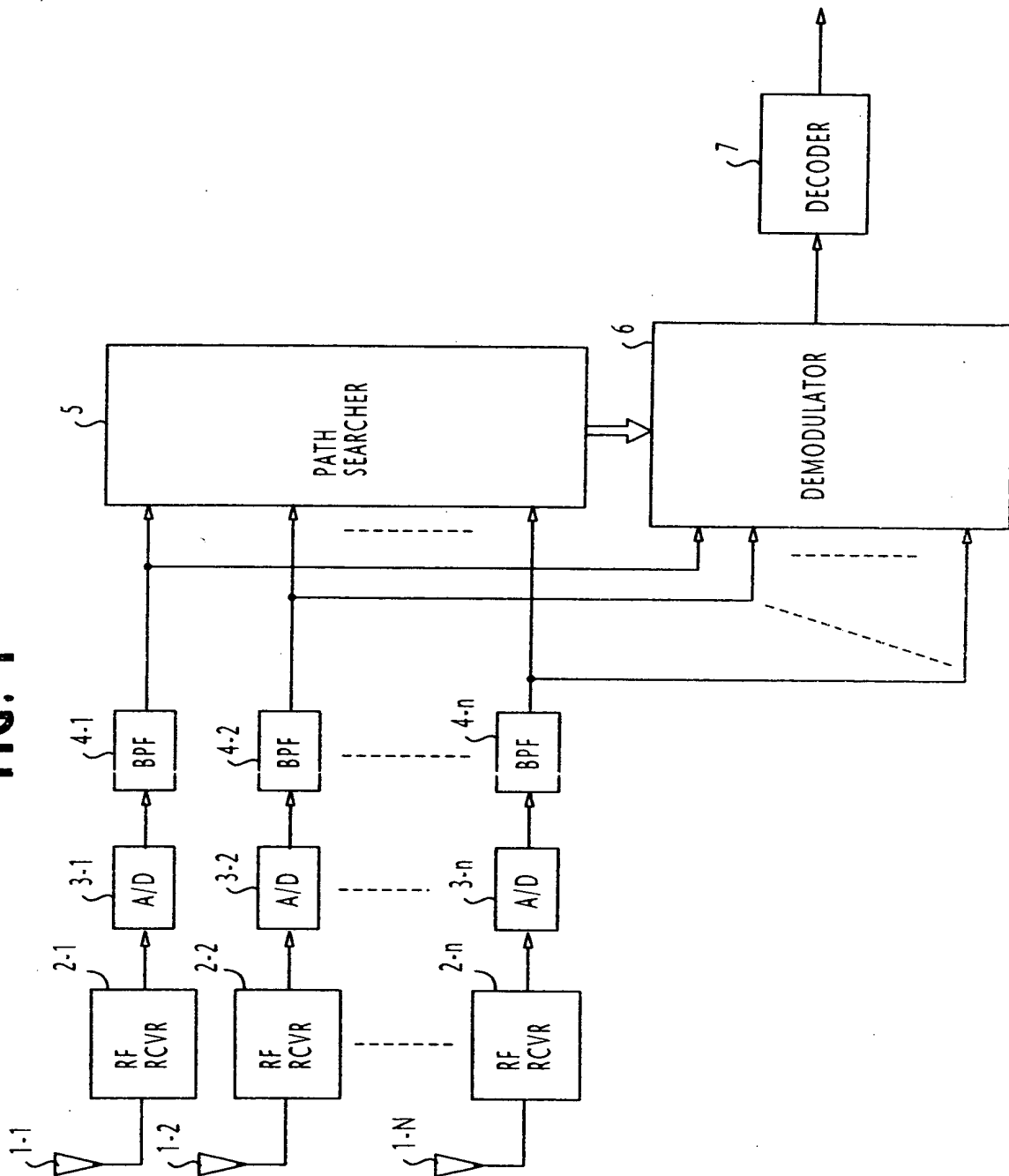


FIG. 2

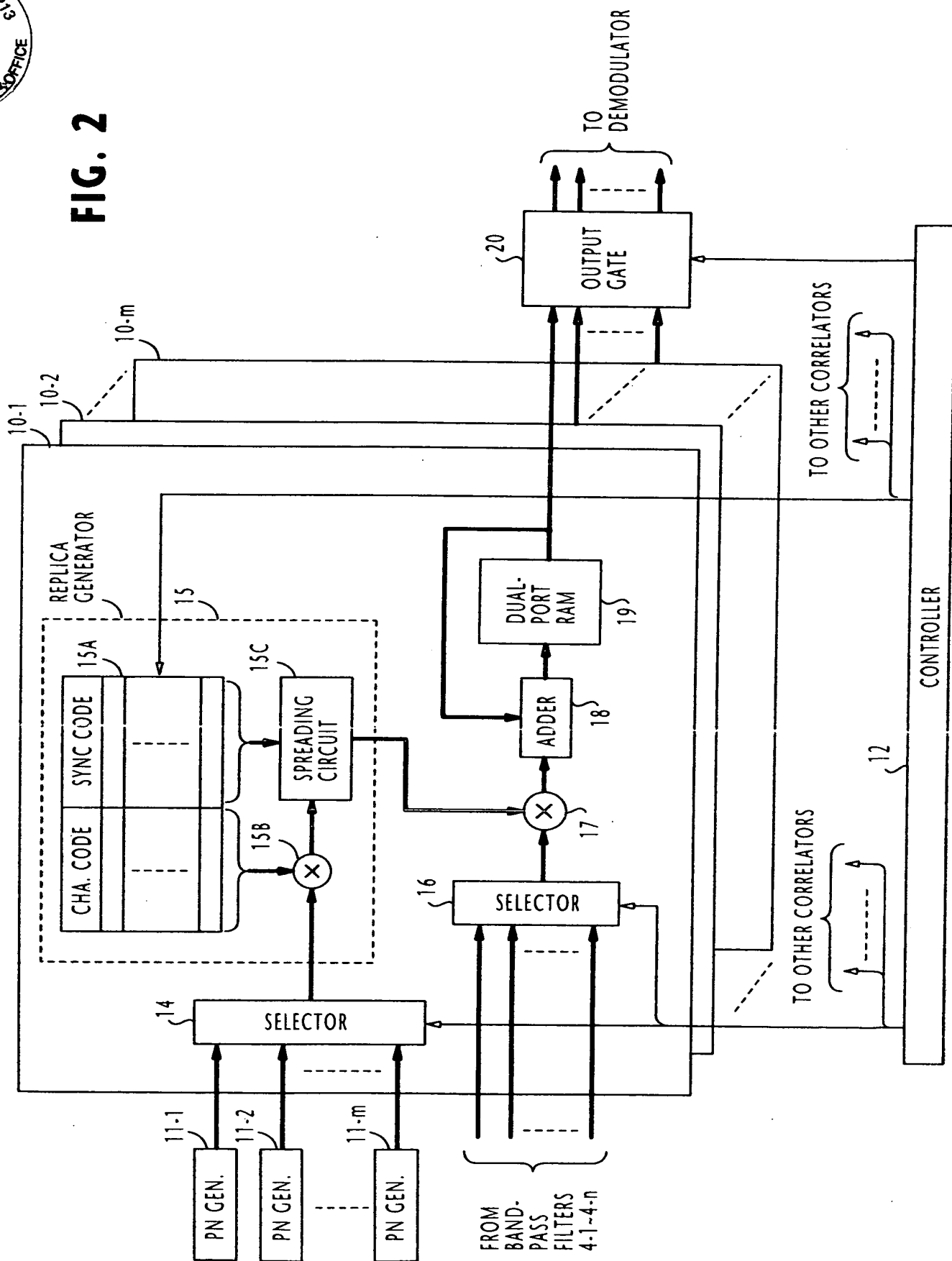
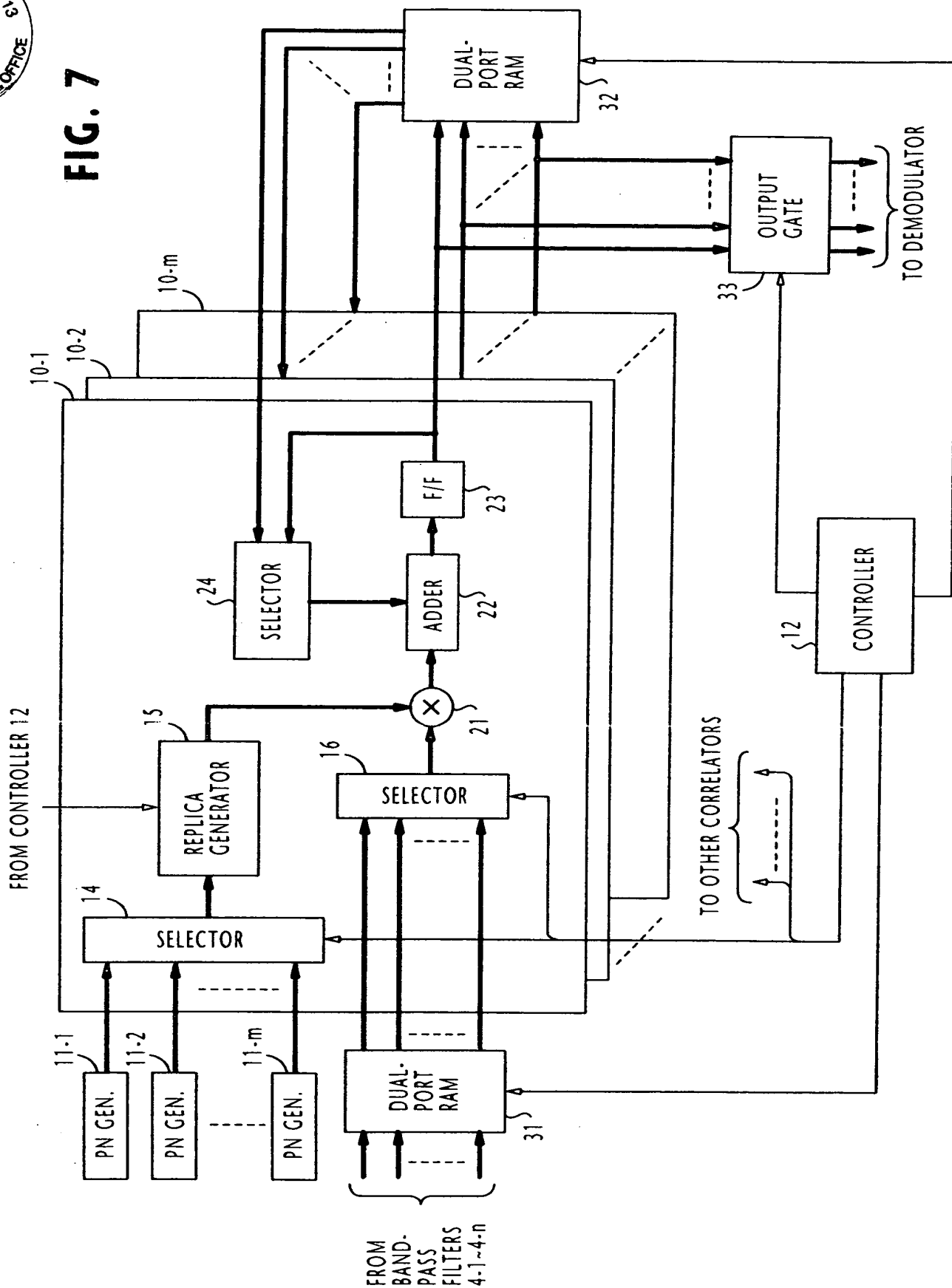


FIG. 1 is a block diagram of a multiplier circuit. The circuit consists of a large block labeled "REPLICA (2,560 CHIPS)" which contains a series of registers labeled R0, R1, ..., R15, ..., R2559. A "SHIFT PULSE (3.84 MHz)" is applied to the left side of the registers. The output of the registers is connected to a series of multipliers labeled Q0, Q1, ..., Q15, ..., Q2559. A "LOAD PULSE (3.84 MHz)" is applied to the right side of the multipliers. The output of the multipliers is connected to a series of adders labeled 43-1, 43-2, ..., 43-16, ..., 43-2559. The output of the adders is connected to a "TO ADDER 18" block. The output of the adders is also connected to a "FROM SELECTOR 16 (3.84 MHz)" block. The output of the selector is connected to a "MULTIPLIER 17" block.

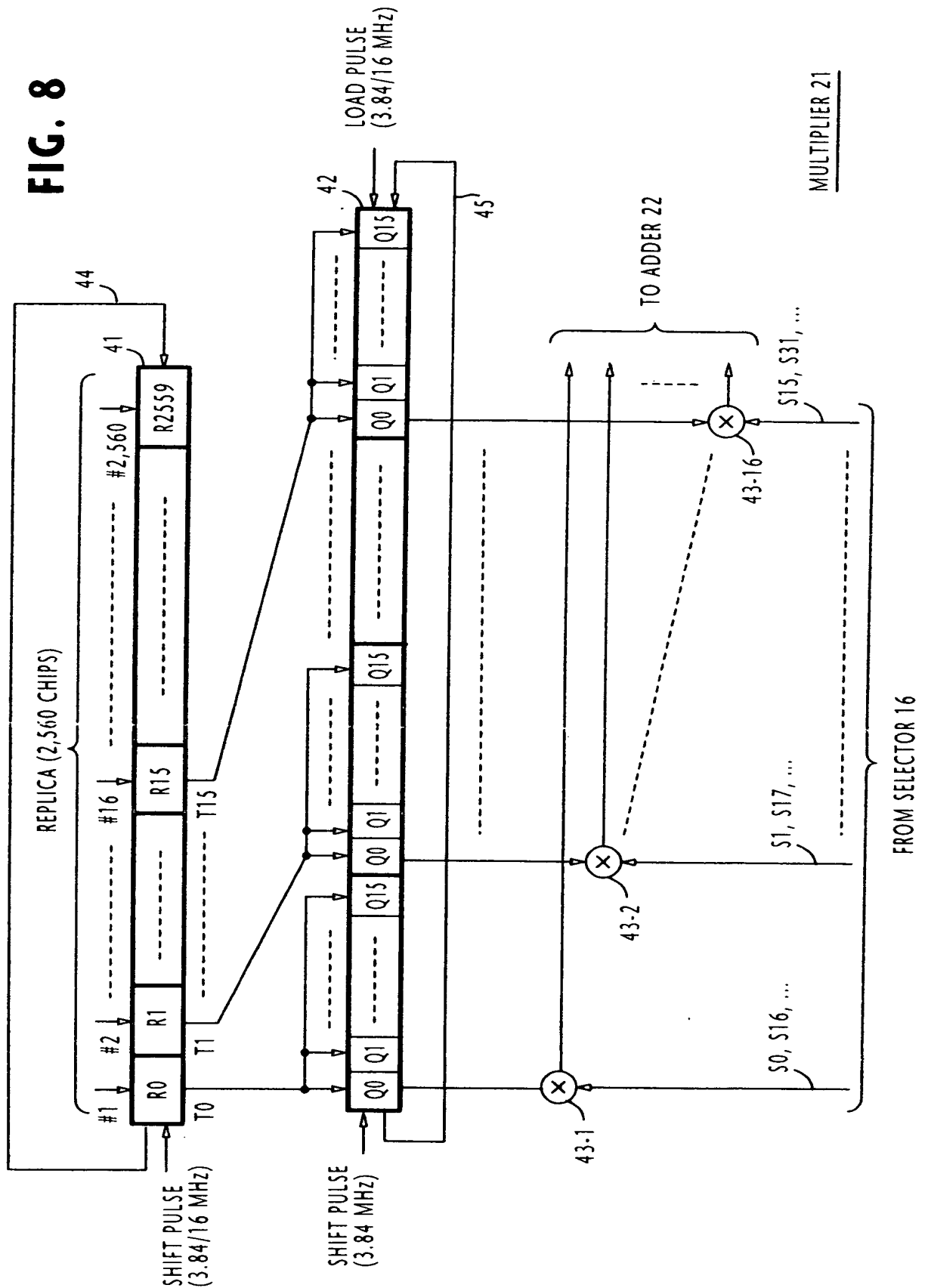


**FIG. 7**





**FIG. 8**



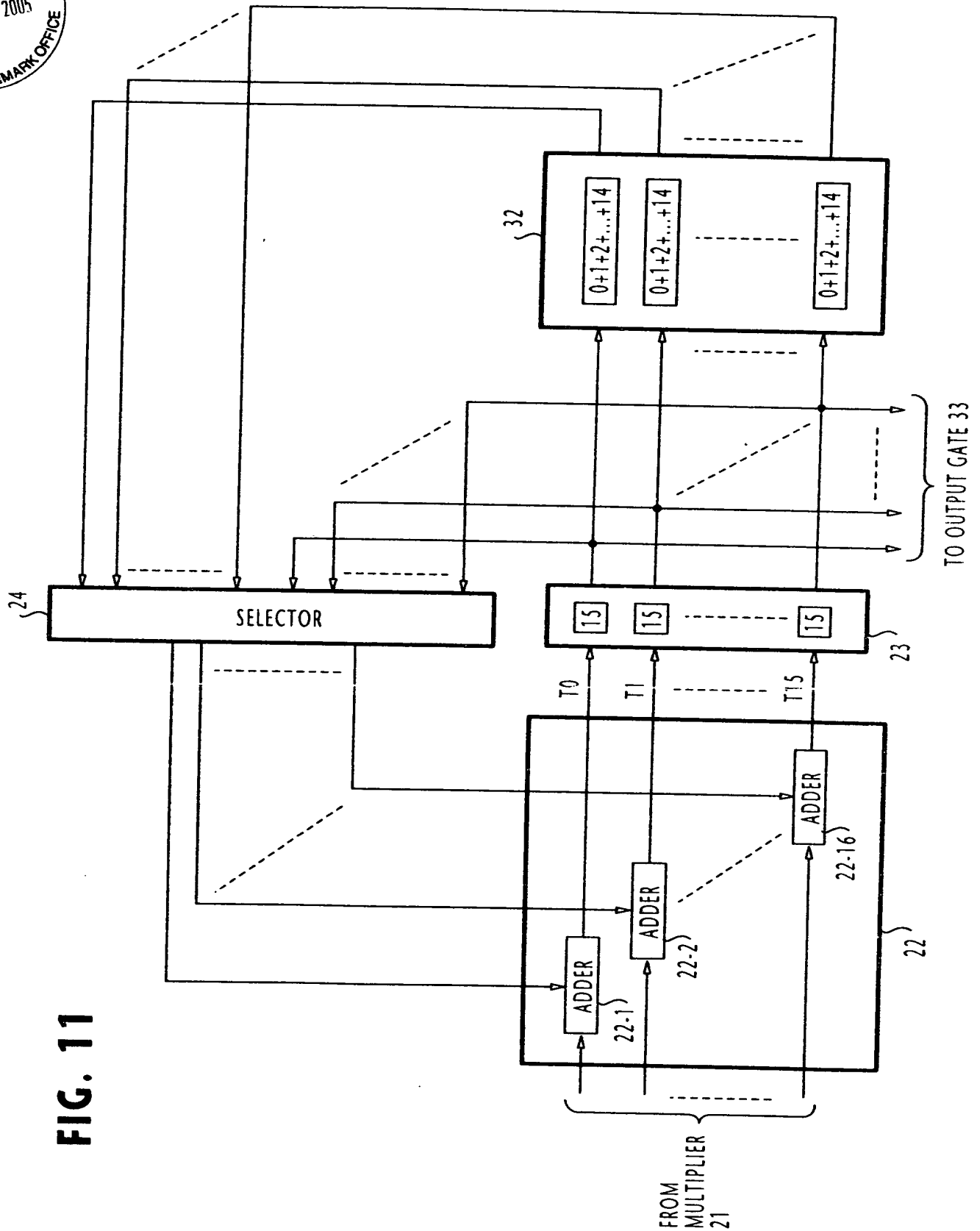


FIG. 11